JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech II SEMESTER(R13/R16) Regular/Supplementary Examinations, MAY-2017.

College: BABA INSTITUTE OF TECHNOLOGY AND SCIENCES:NR

Discrepancy pertaining to these results are to be submitted on or before 20-12-2017 with following documents at CE(PG) Office,JNTUK,Kakinada

Htno	Subcode	Subname	Internal	External	credits
13NR1D0401	H0401	SIMULATION MODELING OF MANUFACTURING SYS	36	-1	0
13NR1D0401	H2103	FINITE ELEMENT METHOD	35	-1	0
13NR1D0411	H0402	COMPUTER GRAPHICS	37	24	1
13NR1D0412	H0401	SIMULATION MODELING OF MANUFACTURING SYS	36	22	0
13NR1D0415	H0401	SIMULATION MODELING OF MANUFACTURING SYS	36	-1	0
13NR1D0418	H0402	COMPUTER GRAPHICS	37	25	1
13NR1D5701	H5701	CAD FOR VLSI	37	28	1
13NR1D5701	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	35	24	1
13NR1D5701	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	36	18	0
13NR1D5704	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	34	19	0
13NR1D5706	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	36	29	1
13NR1D5911	H4002	INFORMATION SECURITY	35	33	1
13NR1D5912	H4002	INFORMATION SECURITY	37	18	0
13NR2D5710	H6809	LOW POWER VLSI DESIGN	36	33	1
13NR2D5910	H4002	INFORMATION SECURITY	35	-1	0
13NR2D5912	H2512	SOFT COMPUTING	35	8	0
13NR2D5912	H4002	INFORMATION SECURITY	35	18	0
13NR2D5912	H5902	COMPUTER SYSTEM ENGINEERING	34	28	1
14NR1D0403	H0402	COMPUTER GRAPHICS	34	24	1
14NR1D0403	H0410	MODELING AND ANALYSIS OF MANUFACTURING P	31	-1	0
14NR1D0403	H1501	OPTIMIZATION AND RELIABILITY	33	10	0
14NR1D0406	H0402	COMPUTER GRAPHICS	35	24	1
14NR1D0409	H0402	COMPUTER GRAPHICS	34	24	1
14NR1D0409	H1501	OPTIMIZATION AND RELIABILITY	32	21	0
14NR1D0410	H1501	OPTIMIZATION AND RELIABILITY	33	12	0
14NR1D0411	H1501	OPTIMIZATION AND RELIABILITY	34	14	0
14NR1D0412	H1501	OPTIMIZATION AND RELIABILITY	32	24	1
14NR1D0413	H0402	COMPUTER GRAPHICS	31	24	1
14NR1D0414	H0402	COMPUTER GRAPHICS	35	24	1
14NR1D5402	H4301	SWITCHED MODE POWER CONVERSION	32	27	1
14NR1D5415	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	34	19	0
14NR1D5713	H5701	CAD FOR VLSI	36	5	0
14NR1D5713	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	32	13	0
14NR1D5714	H5701	CAD FOR VLSI	35	8	0
14NR1D5910	H2512	SOFT COMPUTING	33	0	0
14NR1D5910	H4002	INFORMATION SECURITY	36	12	0
14NR1D5910	H5902	COMPUTER SYSTEM ENGINEERING	34	8	0
14NR1D5913	H2508	CLOUD COMPUTING	36	-1	0
14NR1D5913	H4002	INFORMATION SECURITY	36	3	0
14NR1D5913	H5901	ADVANCED COMPUTER ALGORITHMS	36	1	0
14NR1D5913	H5902	COMPUTER SYSTEM ENGINEERING	35	10	0

Htno	Subcode	Subname	Internal	External	credits
14NR1D5915	H2508	CLOUD COMPUTING	36	14	0
14NR1D5915	H4002	INFORMATION SECURITY	37	19	0
14NR1D5915	H5901	ADVANCED COMPUTER ALGORITHMS	38	27	1
14NR1D5915	H5902	COMPUTER SYSTEM ENGINEERING	37	18	0
14NR1D5918	H4002	INFORMATION SECURITY	34	31	1
14NR2D5408	H4304	CUSTOM POWER DEVICES	37	-1	0
14NR2D5408	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	36	-1	0
14NR2D5411	H4301	SWITCHED MODE POWER CONVERSION	31	-1	0
14NR2D5412	H4303	DIGITAL CONTROLLERS	35	-1	0
14NR2D5412	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	35	-1	0
14NR2D5412	H4308	SPECIAL MACHINES ELECTIVE-IV	35	-1	0
14NR2D5414	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	33	19	0
14NR2D5701	H5701	CAD FOR VLSI	31	0	0
14NR2D5701	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	33	10	0
14NR2D5701	H6809	LOW POWER VLSI DESIGN	33	-1	0
14NR2D5701	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	32	6	0
14NR2D5705	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	34	27	1
14NR2D5712	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	32	19	0
14NR2D5712	H6809	LOW POWER VLSI DESIGN	32	33	1
14NR2D5713	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	36	28	1
14NR2D5716	H5701	CAD FOR VLSI	34	-1	0
14NR2D5716	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	35	-1	0
14NR2D5716	H6809	LOW POWER VLSI DESIGN	37	-1	0
14NR2D5904	H2512	SOFT COMPUTING	33	0	0
14NR2D5904	H4002	INFORMATION SECURITY	35	24	1
14NR2D5905	H4002	INFORMATION SECURITY	36	17	0
14NR2D8705	H8701	FINITE ELEMENT METHOD	36	24	1
14NR2D8705	H8704	THEORY OF PLATES & SHELLS	33	20	0
14NR2D8706	H8701	FINITE ELEMENT METHOD	37	32	1
14NR2D8707	H8701	FINITE ELEMENT METHOD	36	28	1
14NR2D8707	H8703	STABILITY OF STRUCTURES	34	27	1
14NR2D8708	H8701	FINITE ELEMENT METHOD	32	28	1
14NR2D8708	H8703	STABILITY OF STRUCTURES	36	4	0
14NR2D8708	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	33	26	1
14NR2D8710	H8701	FINITE ELEMENT METHOD	36	30	1
14NR2D8710	H8703	STABILITY OF STRUCTURES	34	36	1
14NR2D8710	H8704	THEORY OF PLATES & SHELLS	35	24	1
14NR2D8711	H8704	THEORY OF PLATES & SHELLS	33	15	0
14NR2D8712	H8701	FINITE ELEMENT METHOD	35	24	1
14NR2D8712	H8703	STABILITY OF STRUCTURES	32	13	0
14NR2D8712	H8704	THEORY OF PLATES & SHELLS	32	18	0
14NR2D8712	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	37	24	1
14NR2D8713	H8702	EARTHQUAKE RESISTANT DESIGN	35	26	1
14NR2D8713	H8703	STABILITY OF STRUCTURES	35	24	1
14NR2D8713	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	35	26	1
14NR2D8713	H8711	CAD LAB	36	50	1
14NR2D8716	H8701	FINITE ELEMENT METHOD	36	24	1
14NR2D8716	H8704	THEORY OF PLATES & SHELLS	32	24	1
14NR2D8716	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	35	24	1
14NR2D8718	H8701	FINITE ELEMENT METHOD	32	26	1
14NR2D8718	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	31	24	1

Htno	Subcode	Subname	Internal	External	credits
15NR1D0403	H0402	COMPUTER GRAPHICS	35	31	1
15NR1D0404	H0402	COMPUTER GRAPHICS	31	-1	0
15NR1D0404	H1501	OPTIMIZATION AND RELIABILITY	31	-1	0
15NR1D0404	H2103	FINITE ELEMENT METHOD	33	23	0
15NR1D0405	H0402	COMPUTER GRAPHICS	32	28	1
15NR1D0405	H1501	OPTIMIZATION AND RELIABILITY	35	28	1
15NR1D0408	H0402	COMPUTER GRAPHICS	35	34	1
15NR1D0410	H0402	COMPUTER GRAPHICS	27	24	1
15NR1D0410	H1501	OPTIMIZATION AND RELIABILITY	31	21	0
15NR1D0410	H2103	FINITE ELEMENT METHOD	32	21	0
15NR1D5405	H4301	SWITCHED MODE POWER CONVERSION	34	26	1
15NR1D5405	H4303	DIGITAL CONTROLLERS	32	15	0
15NR1D5405	H4304	CUSTOM POWER DEVICES	33	35	1
15NR1D5405	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	30	10	0
15NR1D5412	H4301	SWITCHED MODE POWER CONVERSION	30	24	1
15NR1D5412	H4303	DIGITAL CONTROLLERS	29	28	1
15NR1D5412	H4304	CUSTOM POWER DEVICES	30	27	1
15NR1D5412	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	28	17	0
15NR1D5707	H5701	CAD FOR VLSI	24	4	0
15NR1D5707	H6804	DESIGN FOR TESTABILITY	28	8	0
15NR1D5707	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	27	0	0
15NR1D5707	H6809	LOW POWER VLSI DESIGN	29	3	0
15NR1D5707	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	13	10	0
15NR1D5710	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	36	14	0
15NR1D5711	H5701	CAD FOR VLSI	34	34	1
15NR1D5711	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	39	9	0
15NR1D5712	H6804	DESIGN FOR TESTABILITY	38	17	0
15NR1D5712	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	36	5	0
15NR1D5712	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	34	11	0
15NR1D5713	H5701	CAD FOR VLSI	29	2	0
15NR1D5713	H6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	29	24	1
15NR1D5713	H6804	DESIGN FOR TESTABILITY	36	6	0
15NR1D5713	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	37	0	0
15NR1D5713	H6809	LOW POWER VLSI DESIGN	19	0	0
15NR1D5713	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	30	0	0
15NR1D5902	H4002	INFORMATION SECURITY	31	26	1
15NR1D5906	H2512	SOFT COMPUTING	33	33	1
15NR1D5906	H4002	INFORMATION SECURITY	32	34	1
15NR1D5906	H5907	CST LAB-2	34	54	1
15NR2D5401	H4301	SWITCHED MODE POWER CONVERSION	36	24	1
15NR2D5401	H4302	ELECTRIC DRIVES-II	32	28	1
15NR2D5403	H4301	SWITCHED MODE POWER CONVERSION	18	-1	0
15NR2D5403	H4302	ELECTRIC DRIVES-II	33	-1	0
15NR2D5403	H4303	DIGITAL CONTROLLERS	0	-1	0
15NR2D5403	H4304	CUSTOM POWER DEVICES	0	4	0
15NR2D5403	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	16	-1	0
15NR2D5403	H4308	SPECIAL MACHINES ELECTIVE-IV	17	-1	0
15NR2D5404	H4302	ELECTRIC DRIVES-II	36	36	1
15NR2D5404	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	33	19	0
15NR2D5410	H4301	SWITCHED MODE POWER CONVERSION	29	9	0
15NR2D5410	H4303	DIGITAL CONTROLLERS	0	6	0

Htno	Subcode	Subname	Internal	External	credits
15NR2D5410	H4304	CUSTOM POWER DEVICES	29	20	0
15NR2D5410	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	29	13	0
15NR2D5410	H4308	SPECIAL MACHINES ELECTIVE-IV	13	24	0
15NR2D5412	H4301	SWITCHED MODE POWER CONVERSION	28	-1	0
15NR2D5412	H4303	DIGITAL CONTROLLERS	29	5	0
15NR2D5412	H4304	CUSTOM POWER DEVICES	29	16	0
15NR2D5412	H4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	28	9	0
15NR2D5413	H4301	SWITCHED MODE POWER CONVERSION	28	13	0
15NR2D5413	H4303	DIGITAL CONTROLLERS	29	8	0
15NR2D5413	H4304	CUSTOM POWER DEVICES	29	19	0
15NR2D5705	H5701	CAD FOR VLSI	27	1	0
15NR2D5705	H6804	DESIGN FOR TESTABILITY	36	6	0
15NR2D5705	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	38	0	0
15NR2D5705	H6809	LOW POWER VLSI DESIGN	31	2	0
15NR2D5705	H6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	27	0	0
15NR2D5901	H2508	CLOUD COMPUTING	33	26	1
15NR2D5901	H2512	SOFT COMPUTING	32	26	1
15NR2D5901	H4001	ADVANCED UNIX PROGRAMMING	33	27	1
15NR2D5901	H4002	INFORMATION SECURITY	34	37	1
15NR2D5901	H5901	ADVANCED COMPUTER ALGORITHMS	32	26	1
15NR2D5901	H5902	COMPUTER SYSTEM ENGINEERING	34	-1	0
15NR2D5902	H2508	CLOUD COMPUTING	33	16	0
15NR2D5902	H4002	INFORMATION SECURITY	32	24	1
15NR2D5902	H5901	ADVANCED COMPUTER ALGORITHMS	32	31	1
15NR2D5903	H2512	SOFT COMPUTING	34	34	1
15NR2D5903	H4002	INFORMATION SECURITY	35	31	1
15NR2D5905	H4002	INFORMATION SECURITY	31	35	1
15NR2D5906	H2508	CLOUD COMPUTING	34	25	1
15NR2D5906	H2512	SOFT COMPUTING	36	26	1
15NR2D5906	H4001	ADVANCED UNIX PROGRAMMING	36	24	1
15NR2D5906	H4002	INFORMATION SECURITY	36	25	1
15NR2D5906	H5901	ADVANCED COMPUTER ALGORITHMS	36	1	0
15NR2D5906	H5902	COMPUTER SYSTEM ENGINEERING	35	12	0
15NR2D8701	H8701	FINITE ELEMENT METHOD	38	24	1
15NR2D8701	H8703	STABILITY OF STRUCTURES	34	26	1
15NR2D8701	H8704	THEORY OF PLATES & SHELLS	37	26	1
15NR2D8701	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	35	24	1
15NR2D8701	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	36	24	1
15NR2D8702	H8701	FINITE ELEMENT METHOD	37	24	1
15NR2D8702	H8702	EARTHQUAKE RESISTANT DESIGN	37	26	1
15NR2D8702	H8703	STABILITY OF STRUCTURES	36	19	0
15NR2D8702	H8704	THEORY OF PLATES & SHELLS	34	24	1
15NR2D8702	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	34	25	1
15NR2D8702	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	33	13	0
15NR2D8705	H8701	FINITE ELEMENT METHOD	34	10	0
15NR2D8705	H8702	EARTHQUAKE RESISTANT DESIGN	36	34	1
15NR2D8705	H8703	STABILITY OF STRUCTURES	36	35	1
15NR2D8705	H8704	THEORY OF PLATES & SHELLS	37	29	1
15NR2D8705	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	35	30	1
15NR2D8705	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	34	26	1
15NR2D8705	H8711	CAD LAB	34	53	1

Htno	Subcode	Subname	Internal	External	credits
15NR2D8707	H8701	FINITE ELEMENT METHOD	38	2	0
15NR2D8707	H8703	STABILITY OF STRUCTURES	34	6	0
15NR2D8707	H8704	THEORY OF PLATES & SHELLS	35	23	0
15NR2D8707	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	33	6	0
15NR2D8707	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	35	12	0
15NR2D8708	H8701	FINITE ELEMENT METHOD	35	1	0
15NR2D8708	H8703	STABILITY OF STRUCTURES	32	18	0
15NR2D8708	H8704	THEORY OF PLATES & SHELLS	36	20	0
15NR2D8708	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	36	24	1
15NR2D8712	H8701	FINITE ELEMENT METHOD	37	28	1
15NR2D8712	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	31	-1	0
15NR2D8714	H8701	FINITE ELEMENT METHOD	37	24	1
15NR2D8714	H8702	EARTHQUAKE RESISTANT DESIGN	32	24	1
15NR2D8714	H8703	STABILITY OF STRUCTURES	36	26	1
15NR2D8714	H8704	THEORY OF PLATES & SHELLS	36	24	1
15NR2D8714	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	31	24	1
15NR2D8714	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	32	24	1
15NR2D8715	H8701	FINITE ELEMENT METHOD	35	2	0
15NR2D8715	H8703	STABILITY OF STRUCTURES	35	24	1
15NR2D8715	H8704	THEORY OF PLATES & SHELLS	34	18	0
15NR2D8715	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	36	26	1
15NR2D8716	H8701	FINITE ELEMENT METHOD	36	1	0
15NR2D8716	H8703	STABILITY OF STRUCTURES	25	0	0
15NR2D8716	H8704	THEORY OF PLATES & SHELLS	28	28	1
15NR2D8716	H8705	PRE-STRESSED CONCRETE ELECTIVE-III	34	8	0
15NR2D8716	H8710	EARTH RETAINING STRUCTURES ELECTIVE-IV	31	9	0
16NR1D0401	J0401	MODELING & SIMULATION OF MANUFACTURING S	17	6	0
16NR1D0401	J0402	COMPUTER GRAPHICS	16	0	0
16NR1D0401	J0405	CONCURRENT ENGINEERING ELECTIVEIII	33	24	1
16NR1D0401	J0407	INTELLIGENT MANUFACTURING SYSTEMS	30	14	0
16NR1D0401	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	27	49	1
16NR1D0401	J1501	OPTIMIZATION AND RELIABILITY	17	0	0
16NR1D0401	J2103	FINITE ELEMENT METHODS	18	8	0
16NR1D0402	J0401	MODELING & SIMULATION OF MANUFACTURING S	34	15	0
16NR1D0402	J0402	COMPUTER GRAPHICS	35	25	1
16NR1D0402	J0405	CONCURRENT ENGINEERING ELECTIVEIII	34	30	1
16NR1D0402	J0407	INTELLIGENT MANUFACTURING SYSTEMS	32	24	1
16NR1D0402	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	28	51	1
16NR1D0402	J1501	OPTIMIZATION AND RELIABILITY	35	16	0
16NR1D0402	J2103	FINITE ELEMENT METHODS	33	13	0
16NR1D0403	J0401	MODELING & SIMULATION OF MANUFACTURING S	37	26	1
16NR1D0403	J0402	COMPUTER GRAPHICS	35	38	1
16NR1D0403	J0405	CONCURRENT ENGINEERING ELECTIVEIII	36	47	1
16NR1D0403	J0407	INTELLIGENT MANUFACTURING SYSTEMS	34	36	1
16NR1D0403	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	26	50	1
16NR1D0403	J1501	OPTIMIZATION AND RELIABILITY	34	24	1
16NR1D0403	J2103	FINITE ELEMENT METHODS	33	17	0
16NR1D0404	J0401	MODELING & SIMULATION OF MANUFACTURING S	34	13	0
16NR1D0404	J0402	COMPUTER GRAPHICS	37	15	0
16NR1D0404	J0405	CONCURRENT ENGINEERING ELECTIVEIII	34	24	1
16NR1D0404	J0407	INTELLIGENT MANUFACTURING SYSTEMS	35	26	1

Htno	Subcode	Subname	Internal	External	credits
16NR1D0404	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	31	55	1
16NR1D0404	J1501	OPTIMIZATION AND RELIABILITY	37	0	0
16NR1D0404	J2103	FINITE ELEMENT METHODS	35	6	0
16NR1D0405	J0401	MODELING & SIMULATION OF MANUFACTURING S	0	-1	0
16NR1D0405	J0402	COMPUTER GRAPHICS	0	-1	0
16NR1D0405	J0405	CONCURRENT ENGINEERING ELECTIVEIII	0	-1	0
16NR1D0405	J0407	INTELLIGENT MANUFACTURING SYSTEMS	0	-1	0
16NR1D0405	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	15	-1	0
16NR1D0405	J1501	OPTIMIZATION AND RELIABILITY	0	-1	0
16NR1D0405	J2103	FINITE ELEMENT METHODS	0	-1	0
16NR1D0406	J0401	MODELING & SIMULATION OF MANUFACTURING S	33	17	0
16NR1D0406	J0402	COMPUTER GRAPHICS	35	26	1
16NR1D0406	J0405	CONCURRENT ENGINEERING ELECTIVEIII	31	37	1
16NR1D0406	J0407	INTELLIGENT MANUFACTURING SYSTEMS	33	26	1
16NR1D0406	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	29	54	1
16NR1D0406	J1501	OPTIMIZATION AND RELIABILITY	33	24	1
16NR1D0406	J2103	FINITE ELEMENT METHODS	33	4	0
16NR1D0407	J0401	MODELING & SIMULATION OF MANUFACTURING S	35	24	1
16NR1D0407	J0402	COMPUTER GRAPHICS	33	29	1
16NR1D0407	J0405	CONCURRENT ENGINEERING ELECTIVEIII	34	41	1
16NR1D0407	J0407	INTELLIGENT MANUFACTURING SYSTEMS	33	28	1
16NR1D0407	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	28	52	1
16NR1D0407	J1501	OPTIMIZATION AND RELIABILITY	34	24	1
16NR1D0407	J2103	FINITE ELEMENT METHODS	33	6	0
16NR1D0408	J0401	MODELING & SIMULATION OF MANUFACTURING S	33	-1	0
16NR1D0408	J0402	COMPUTER GRAPHICS	18	-1	0
16NR1D0408	J0405	CONCURRENT ENGINEERING ELECTIVEIII	30	-1	0
16NR1D0408	J0407	INTELLIGENT MANUFACTURING SYSTEMS	32	-1	0
16NR1D0408	J0408	MODELING AND ANALYSIS OF MANUFACTURING P	30	53	1
16NR1D0408	J1501	OPTIMIZATION AND RELIABILITY	34	-1	0
16NR1D0408	J2103	FINITE ELEMENT METHODS	35	-1	0
16NR1D5401	J4301	SWITCHED MODE POWER CONVERSION	0	-1	0
16NR1D5401	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	0	-1	0
16NR1D5401	J4303	DIGITAL CONTROLLERS	0	-1	0
16NR1D5401	J4304	CUSTOM POWER DEVICES	0	-1	0
16NR1D5401	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	0	-1	0
16NR1D5401	J4308	SPECIAL MACHINES ELECTIVEIV	0	-1	0
16NR1D5401	J4310	POWER CONVERTERS & DRIVES LABORATORY	0	-1	0
16NR1D5402	J4301	SWITCHED MODE POWER CONVERSION	35	41	1
16NR1D5402	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	35	27	1
16NR1D5402	J4303	DIGITAL CONTROLLERS	33	30	1
16NR1D5402	J4304	CUSTOM POWER DEVICES	36	29	1
16NR1D5402	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	38	24	1
16NR1D5402	J4308	SPECIAL MACHINES ELECTIVEIV	39	27	1
16NR1D5402	J4310	POWER CONVERTERS & DRIVES LABORATORY	39	56	1
16NR1D5403	J4301	SWITCHED MODE POWER CONVERSION	35	37	1
16NR1D5403	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	33	33	1
16NR1D5403	J4303	DIGITAL CONTROLLERS	34	8	0
16NR1D5403	J4304	CUSTOM POWER DEVICES	34	31	1
16NR1D5403	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	36	25	1
16NR1D5403	J4308	SPECIAL MACHINES ELECTIVEIV	36	-1	0

Htno	Subcode	Subname	Internal	External	credits
16NR1D5403	J4310	POWER CONVERTERS & DRIVES LABORATORY	37	52	1
16NR1D5404	J4301	SWITCHED MODE POWER CONVERSION	20	30	1
16NR1D5404	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	18	13	0
16NR1D5404	J4303	DIGITAL CONTROLLERS	16	26	0
16NR1D5404	J4304	CUSTOM POWER DEVICES	16	11	0
16NR1D5404	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	17	15	0
16NR1D5404	J4308	SPECIAL MACHINES ELECTIVEIV	18	15	0
16NR1D5404	J4310	POWER CONVERTERS & DRIVES LABORATORY	35	49	1
16NR1D5405	J4301	SWITCHED MODE POWER CONVERSION	30	34	1
16NR1D5405	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	34	24	1
16NR1D5405	J4303	DIGITAL CONTROLLERS	32	27	1
16NR1D5405	J4304	CUSTOM POWER DEVICES	34	36	1
16NR1D5405	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	35	24	1
16NR1D5405	J4308	SPECIAL MACHINES ELECTIVEIV	35	24	1
16NR1D5405	J4310	POWER CONVERTERS & DRIVES LABORATORY	37	50	1
16NR1D5406	J4301	SWITCHED MODE POWER CONVERSION	32	5	0
16NR1D5406	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	33	12	0
16NR1D5406	J4303	DIGITAL CONTROLLERS	33	25	1
16NR1D5406	J4304	CUSTOM POWER DEVICES	34	14	0
16NR1D5406	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	29	13	0
16NR1D5406	J4308	SPECIAL MACHINES ELECTIVEIV	36	24	1
16NR1D5406	J4310	POWER CONVERTERS & DRIVES LABORATORY	38	50	1
16NR1D5407	J4301	SWITCHED MODE POWER CONVERSION	0	-1	0
16NR1D5407	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	0	-1	0
16NR1D5407	J4303	DIGITAL CONTROLLERS	0	-1	0
16NR1D5407	J4304	CUSTOM POWER DEVICES	0	-1	0
16NR1D5407	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	0	-1	0
16NR1D5407	J4308	SPECIAL MACHINES ELECTIVEIV	0	-1	0
16NR1D5407	J4310	POWER CONVERTERS & DRIVES LABORATORY	0	-1	0
16NR1D5408	J4301	SWITCHED MODE POWER CONVERSION	30	0	0
16NR1D5408	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	33	0	0
16NR1D5408	J4303	DIGITAL CONTROLLERS	33	26	1
16NR1D5408	J4304	CUSTOM POWER DEVICES	33	29	1
16NR1D5408	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	33	24	1
16NR1D5408	J4308	SPECIAL MACHINES ELECTIVEIV	36	24	1
16NR1D5408	J4310	POWER CONVERTERS & DRIVES LABORATORY	37	52	1
16NR1D5701	J5704	BACK END VLSI DESIGN LABORATORY	37	56	1
16NR1D5701	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	34	25	1
16NR1D5701	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	33	31	1
16NR1D5701	J6804	DESIGN FOR TESTABILITY	35	18	0
16NR1D5701	J6805	DSP PROCESSORS AND ARCHITECTURES	36	24	1
16NR1D5701	J6806	LOW POWER VLSI DESIGN	32	26	1
16NR1D5701	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	35	14	0
16NR1D5702	J5704	BACK END VLSI DESIGN LABORATORY	0	-1	0
16NR1D5702	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	0	-1	0
16NR1D5702	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	0	-1	0
16NR1D5702	J6804	DESIGN FOR TESTABILITY	0	-1	0
16NR1D5702	J6805	DSP PROCESSORS AND ARCHITECTURES	0	-1	0
16NR1D5702	J6806	LOW POWER VLSI DESIGN	0	-1	0
16NR1D5702	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	0	-1	0
16NR1D5703	J5704	BACK END VLSI DESIGN LABORATORY	37	54	1

Htno	Subcode	Subname	Internal	External	credits
16NR1D5703	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	34	33	1
16NR1D5703	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	34	40	1
16NR1D5703	J6804	DESIGN FOR TESTABILITY	35	27	1
16NR1D5703	J6805	DSP PROCESSORS AND ARCHITECTURES	35	37	1
16NR1D5703	J6806	LOW POWER VLSI DESIGN	34	35	1
16NR1D5703	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	32	26	1
16NR1D5704	J5704	BACK END VLSI DESIGN LABORATORY	38	55	1
16NR1D5704	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	35	31	1
16NR1D5704	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	36	27	1
16NR1D5704	J6804	DESIGN FOR TESTABILITY	36	24	1
16NR1D5704	J6805	DSP PROCESSORS AND ARCHITECTURES	35	30	1
16NR1D5704	J6806	LOW POWER VLSI DESIGN	36	32	1
16NR1D5704	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	35	16	0
16NR1D5705	J5704	BACK END VLSI DESIGN LABORATORY	0	-1	0
16NR1D5705	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	0	-1	0
16NR1D5705	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	0	-1	0
16NR1D5705	J6804	DESIGN FOR TESTABILITY	0	-1	0
16NR1D5705	J6805	DSP PROCESSORS AND ARCHITECTURES	0	-1	0
16NR1D5705	J6806	LOW POWER VLSI DESIGN	0	-1	0
16NR1D5705	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	0	-1	0
16NR1D5706	J5704	BACK END VLSI DESIGN LABORATORY	36	41	1
16NR1D5706	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	36	14	0
16NR1D5706	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	36	33	1
16NR1D5706	J6804	DESIGN FOR TESTABILITY	35	5	0
16NR1D5706	J6805	DSP PROCESSORS AND ARCHITECTURES	36	25	1
16NR1D5706	J6806	LOW POWER VLSI DESIGN	36	9	0
16NR1D5706	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	34	0	0
16NR1D5901	J0504	COMPILER DESIGN ELECTIVE I	35	38	1
16NR1D5901	J2512	INTERNET OF THINGS ELECTIVE II	34	33	1
16NR1D5901	J4001	ADVANCED UNIX PROGRAMMING	34	28	1
16NR1D5901	J4002	BIG DATA ANALYTICS	37	29	1
16NR1D5901	J5901	PYTHON PROGRAMMING	39	48	1
16NR1D5901	J5905	CST LAB 2	36	58	1
16NR1D5901	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	34	32	1
16NR1D5902	J0504	COMPILER DESIGN ELECTIVE I	36	44	1
16NR1D5902	J2512	INTERNET OF THINGS ELECTIVE II	36	-1	0
16NR1D5902	J4001	ADVANCED UNIX PROGRAMMING	37	-1	0
16NR1D5902	J4002	BIG DATA ANALYTICS	37	38	1
16NR1D5902	J5901	PYTHON PROGRAMMING	39	48	1
16NR1D5902	J5905	CST LAB 2	38	59	1
16NR1D5902	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	33	35	1
16NR1D5903	J0504	COMPILER DESIGN ELECTIVE I	20	10	0
16NR1D5903	J2512	INTERNET OF THINGS ELECTIVE II	17	1	0
16NR1D5903	J4001	ADVANCED UNIX PROGRAMMING	18	24	0
16NR1D5903	J4002	BIG DATA ANALYTICS	19	31	1
16NR1D5903	J5901	PYTHON PROGRAMMING	20	32	1
16NR1D5903	J5905	CST LAB 2	36	58	1
16NR1D5903	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	19	11	0
16NR1D5904	J0504	COMPILER DESIGN ELECTIVE I	29	38	1
16NR1D5904	J2512	INTERNET OF THINGS ELECTIVE II	31	35	1
16NR1D5904	J4001	ADVANCED UNIX PROGRAMMING	38	33	1

Htno	Subcode	Subname	Internal	External	credits
16NR1D5904	J4002	BIG DATA ANALYTICS	31	-1	0
16NR1D5904	J5901	PYTHON PROGRAMMING	33	-1	0
16NR1D5904	J5905	CST LAB 2	36	57	1
16NR1D5904	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	31	26	1
16NR1D5905	J0504	COMPILER DESIGN ELECTIVE I	34	44	1
16NR1D5905	J2512	INTERNET OF THINGS ELECTIVE II	33	33	1
16NR1D5905	J4001	ADVANCED UNIX PROGRAMMING	34	24	1
16NR1D5905	J4002	BIG DATA ANALYTICS	36	32	1
16NR1D5905	J5901	PYTHON PROGRAMMING	38	44	1
16NR1D5905	J5905	CST LAB 2	37	58	1
16NR1D5905	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	32	25	1
16NR1D5906	J0504	COMPILER DESIGN ELECTIVE I	0	-1	0
16NR1D5906	J2512	INTERNET OF THINGS ELECTIVE II	0	-1	0
16NR1D5906	J4001	ADVANCED UNIX PROGRAMMING	0	-1	0
16NR1D5906	J4002	BIG DATA ANALYTICS	0	-1	0
16NR1D5906	J5901	PYTHON PROGRAMMING	0	-1	0
16NR1D5906	J5905	CST LAB 2	0	-1	0
16NR1D5906	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	0	-1	0
16NR1D5907	J0504	COMPILER DESIGN ELECTIVE I	0	-1	0
16NR1D5907	J2512	INTERNET OF THINGS ELECTIVE II	0	-1	0
16NR1D5907	J4001	ADVANCED UNIX PROGRAMMING	0	-1	0
16NR1D5907	J4002	BIG DATA ANALYTICS	0	-1	0
16NR1D5907	J5901	PYTHON PROGRAMMING	0	-1	0
16NR1D5907	J5905	CST LAB 2	0	-1	0
16NR1D5907	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	0	-1	0
16NR1D5908	J0504	COMPILER DESIGN ELECTIVE I	35	32	1
16NR1D5908	J2512	INTERNET OF THINGS ELECTIVE II	32	32	1
16NR1D5908	J4001	ADVANCED UNIX PROGRAMMING	35	24	1
16NR1D5908	J4002	BIG DATA ANALYTICS	37	36	1
16NR1D5908	J5901	PYTHON PROGRAMMING	37	48	1
16NR1D5908	J5905	CST LAB 2	37	58	1
16NR1D5908	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	35	27	1
16NR1D5909	J0504	COMPILER DESIGN ELECTIVE I	34	-1	0
16NR1D5909	J2512	INTERNET OF THINGS ELECTIVE II	36	-1	0
16NR1D5909	J4001	ADVANCED UNIX PROGRAMMING	37	-1	0
16NR1D5909	J4002	BIG DATA ANALYTICS	36	-1	0
16NR1D5909	J5901	PYTHON PROGRAMMING	39	-1	0
16NR1D5909	J5905	CST LAB 2	0	-1	0
16NR1D5909	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	29	-1	0
16NR1D5910	J0504	COMPILER DESIGN ELECTIVE I	34	14	0
16NR1D5910	J2512	INTERNET OF THINGS ELECTIVE II	29	29	1
16NR1D5910	J4001	ADVANCED UNIX PROGRAMMING	38	13	0
16NR1D5910	J4002	BIG DATA ANALYTICS	35	26	1
16NR1D5910	J5901	PYTHON PROGRAMMING	40	40	1
16NR1D5910	J5905	CST LAB 2	36	59	1
16NR1D5910	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	32	25	1
16NR1D5911	J0504	COMPILER DESIGN ELECTIVE I	33	24	1
16NR1D5911	J2512	INTERNET OF THINGS ELECTIVE II	30	32	1
16NR1D5911	J4001	ADVANCED UNIX PROGRAMMING	34	14	0
16NR1D5911	J4002	BIG DATA ANALYTICS	37	32	1
16NR1D5911	J5901	PYTHON PROGRAMMING	38	36	1

Htno	Subcode	Subname	Internal	External	credits
16NR1D5911	J5905	CST LAB 2	37	59	1
16NR1D5911	J8405	ADVANCED COMPUTER ARCHITECTURE ELECTIVE	30	25	1
16NR2D5401	J4301	SWITCHED MODE POWER CONVERSION	30	35	1
16NR2D5401	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	31	32	1
16NR2D5401	J4303	DIGITAL CONTROLLERS	31	28	1
16NR2D5401	J4304	CUSTOM POWER DEVICES	34	27	1
16NR2D5401	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	32	24	1
16NR2D5401	J4308	SPECIAL MACHINES ELECTIVEIV	33	28	1
16NR2D5401	J4310	POWER CONVERTERS & DRIVES LABORATORY	33	50	1
16NR2D5402	J4301	SWITCHED MODE POWER CONVERSION	36	38	1
16NR2D5402	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	36	38	1
16NR2D5402	J4303	DIGITAL CONTROLLERS	33	35	1
16NR2D5402	J4304	CUSTOM POWER DEVICES	36	39	1
16NR2D5402	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	35	24	1
16NR2D5402	J4308	SPECIAL MACHINES ELECTIVEIV	39	41	1
16NR2D5402	J4310	POWER CONVERTERS & DRIVES LABORATORY	39	56	1
16NR2D5403	J4301	SWITCHED MODE POWER CONVERSION	31	27	1
16NR2D5403	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	34	29	1
16NR2D5403	J4303	DIGITAL CONTROLLERS	32	4	0
16NR2D5403	J4304	CUSTOM POWER DEVICES	33	17	0
16NR2D5403	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	35	24	1
16NR2D5403	J4308	SPECIAL MACHINES ELECTIVEIV	37	24	1
16NR2D5403	J4310	POWER CONVERTERS & DRIVES LABORATORY	38	55	1
16NR2D5404	J4301	SWITCHED MODE POWER CONVERSION	0	-1	0
16NR2D5404	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	0	-1	0
16NR2D5404	J4303	DIGITAL CONTROLLERS	0	-1	0
16NR2D5404	J4304	CUSTOM POWER DEVICES	0	-1	0
16NR2D5404	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	0	-1	0
16NR2D5404	J4308	SPECIAL MACHINES ELECTIVEIV	0	-1	0
16NR2D5404	J4310	POWER CONVERTERS & DRIVES LABORATORY	0	-1	0
16NR2D5405	J4301	SWITCHED MODE POWER CONVERSION	0	-1	0
16NR2D5405	J4302	POWER ELECTRONIC CONTROL OF AC DRIVES	0	-1	0
16NR2D5405	J4303	DIGITAL CONTROLLERS	0	-1	0
16NR2D5405	J4304	CUSTOM POWER DEVICES	0	-1	0
16NR2D5405	J4307	ELECTRICAL DISTRIBUTION SYSTEMS ELECTIVE	0	-1	0
16NR2D5405	J4308	SPECIAL MACHINES ELECTIVEIV	0	-1	0
16NR2D5405	J4310	POWER CONVERTERS & DRIVES LABORATORY	0	-1	0
16NR2D5701	J5704	BACK END VLSI DESIGN LABORATORY	36	53	1
16NR2D5701	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	33	36	1
16NR2D5701	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	36	45	1
16NR2D5701	J6804	DESIGN FOR TESTABILITY	37	27	1
16NR2D5701	J6805	DSP PROCESSORS AND ARCHITECTURES	36	44	1
16NR2D5701	J6806	LOW POWER VLSI DESIGN	34	42	1
16NR2D5701	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	32	25	1
16NR2D5702	J5704	BACK END VLSI DESIGN LABORATORY	37	51	1
16NR2D5702	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	34	-1	0
16NR2D5702	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	35	28	1
16NR2D5702	J6804	DESIGN FOR TESTABILITY	34	6	0
16NR2D5702	J6805	DSP PROCESSORS AND ARCHITECTURES	35	10	0
16NR2D5702	J6806	LOW POWER VLSI DESIGN	34	13	0
16NR2D5702	J6810	SEMICONDUCTOR MEMORY DESIGN AND TESTING	28	0	0

Htno	Subcode	Subname	Internal	External	credits
16NR2D8701	J8701	FINITE ELEMENT METHODS	0	-1	0
16NR2D8701	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	0	-1	0
16NR2D8701	J8703	STABILITY OF STRUCTURES	0	-1	0
16NR2D8701	J8704	THEORY OF PLATES & SHELLS	0	-1	0
16NR2D8701	J8705	PRESTRESSED CONCRETE ELECTIVEI	0	-1	0
16NR2D8701	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	0	-1	0
16NR2D8701	J8711	CAD LABORATORY	0	-1	0
16NR2D8702	J8701	FINITE ELEMENT METHODS	32	30	1
16NR2D8702	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	29	29	1
16NR2D8702	J8703	STABILITY OF STRUCTURES	34	24	1
16NR2D8702	J8704	THEORY OF PLATES & SHELLS	30	16	0
16NR2D8702	J8705	PRESTRESSED CONCRETE ELECTIVEI	31	29	1
16NR2D8702	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	32	24	1
16NR2D8702	J8711	CAD LABORATORY	34	48	1
16NR2D8703	J8701	FINITE ELEMENT METHODS	33	24	1
16NR2D8703	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	32	25	1
16NR2D8703	J8703	STABILITY OF STRUCTURES	36	24	1
16NR2D8703	J8704	THEORY OF PLATES & SHELLS	34	24	1
16NR2D8703	J8705	PRESTRESSED CONCRETE ELECTIVEI	33	24	1
16NR2D8703	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	34	24	1
16NR2D8703	J8711	CAD LABORATORY	36	50	1
16NR2D8704	J8701	FINITE ELEMENT METHODS	36	25	1
16NR2D8704	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	35	12	0
16NR2D8704	J8703	STABILITY OF STRUCTURES	38	24	1
16NR2D8704	J8704	THEORY OF PLATES & SHELLS	35	10	0
16NR2D8704	J8705	PRESTRESSED CONCRETE ELECTIVEI	36	26	1
16NR2D8704	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	38	27	1
16NR2D8704	J8711	CAD LABORATORY	38	54	1
16NR2D8705	J8701	FINITE ELEMENT METHODS	0	-1	0
16NR2D8705	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	0	-1	0
16NR2D8705	J8703	STABILITY OF STRUCTURES	0	-1	0
16NR2D8705	J8704	THEORY OF PLATES & SHELLS	0	-1	0
16NR2D8705	J8705	PRESTRESSED CONCRETE ELECTIVEI	0	-1	0
16NR2D8705	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	0	-1	0
16NR2D8705	J8711	CAD LABORATORY	0	-1	0
16NR2D8706	J8701	FINITE ELEMENT METHODS	34	30	1
16NR2D8706	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	35	27	1
16NR2D8706	J8703	STABILITY OF STRUCTURES	35	27	1
16NR2D8706	J8704	THEORY OF PLATES & SHELLS	33	16	0
16NR2D8706	J8705	PRESTRESSED CONCRETE ELECTIVEI	36	25	1
16NR2D8706	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	36	25	1
16NR2D8706	J8711	CAD LABORATORY	32	50	1
16NR2D8707	J8701	FINITE ELEMENT METHODS	30	34	1
16NR2D8707	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	30	32	1
16NR2D8707	J8703	STABILITY OF STRUCTURES	31	24	1
16NR2D8707	J8704	THEORY OF PLATES & SHELLS	34	29	1
16NR2D8707	J8705	PRESTRESSED CONCRETE ELECTIVEI	30	30	1
16NR2D8707	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	34	30	1
16NR2D8707	J8711	CAD LABORATORY	30	50	1
16NR2D8708	J8701	FINITE ELEMENT METHODS	37	33	1
16NR2D8708	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	33	27	1

Htno	Subcode	Subname	Internal	External	credits
16NR2D8708	J8703	STABILITY OF STRUCTURES	37	27	1
16NR2D8708	J8704	THEORY OF PLATES & SHELLS	34	24	1
16NR2D8708	J8705	PRESTRESSED CONCRETE ELECTIVEI	37	27	1
16NR2D8708	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	38	34	1
16NR2D8708	J8711	CAD LABORATORY	36	53	1
16NR2D8709	J8701	FINITE ELEMENT METHODS	37	18	0
16NR2D8709	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	35	28	1
16NR2D8709	J8703	STABILITY OF STRUCTURES	37	18	0
16NR2D8709	J8704	THEORY OF PLATES & SHELLS	37	0	0
16NR2D8709	J8705	PRESTRESSED CONCRETE ELECTIVEI	34	8	0
16NR2D8709	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	38	8	0
16NR2D8709	J8711	CAD LABORATORY	36	54	1
16NR2D8710	J8701	FINITE ELEMENT METHODS	36	43	1
16NR2D8710	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	35	31	1
16NR2D8710	J8703	STABILITY OF STRUCTURES	37	40	1
16NR2D8710	J8704	THEORY OF PLATES & SHELLS	36	24	1
16NR2D8710	J8705	PRESTRESSED CONCRETE ELECTIVEI	32	29	1
16NR2D8710	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	36	43	1
16NR2D8710	J8711	CAD LABORATORY	38	53	1
16NR2D8711	J8701	FINITE ELEMENT METHODS	35	25	1
16NR2D8711	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	33	33	1
16NR2D8711	J8703	STABILITY OF STRUCTURES	36	25	1
16NR2D8711	J8704	THEORY OF PLATES & SHELLS	32	24	1
16NR2D8711	J8705	PRESTRESSED CONCRETE ELECTIVEI	35	31	1
16NR2D8711	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	36	38	1
16NR2D8711	J8711	CAD LABORATORY	34	51	1
16NR2D8712	J8701	FINITE ELEMENT METHODS	33	33	1
16NR2D8712	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	32	26	1
16NR2D8712	J8703	STABILITY OF STRUCTURES	33	29	1
16NR2D8712	J8704	THEORY OF PLATES & SHELLS	33	25	1
16NR2D8712	J8705	PRESTRESSED CONCRETE ELECTIVEI	31	30	1
16NR2D8712	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	34	44	1
16NR2D8712	J8711	CAD LABORATORY	32	-1	0
16NR2D8713	J8701	FINITE ELEMENT METHODS	36	38	1
16NR2D8713	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	33	33	1
16NR2D8713	J8703	STABILITY OF STRUCTURES	35	35	1
16NR2D8713	J8704	THEORY OF PLATES & SHELLS	33	11	0
16NR2D8713	J8705	PRESTRESSED CONCRETE ELECTIVEI	37	29	1
16NR2D8713	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	35	24	1
16NR2D8713	J8711	CAD LABORATORY	34	51	1
16NR2D8714	J8701	FINITE ELEMENT METHODS	32	24	1
16NR2D8714	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	33	16	0
16NR2D8714	J8703	STABILITY OF STRUCTURES	34	24	1
16NR2D8714	J8704	THEORY OF PLATES & SHELLS	32	3	0
16NR2D8714	J8705	PRESTRESSED CONCRETE ELECTIVEI	32	24	1
16NR2D8714	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	32	13	0
16NR2D8714	J8711	CAD LABORATORY	36	51	1
16NR2D8715	J8701	FINITE ELEMENT METHODS	32	17	0
16NR2D8715	J8702	EARTHQUAKE RESISTANT STRUCTURES ELECTIVE	32	0	0
16NR2D8715	J8703	STABILITY OF STRUCTURES	34	19	0
16NR2D8715	J8704	THEORY OF PLATES & SHELLS	32	4	0

Htno	Subcode	Subname	Internal	External	credits
16NR2D8715	J8705	PRESTRESSED CONCRETE ELECTIVEI	33	24	1
16NR2D8715	J8710	EARTH RETAINING STRUCTURES ELECTIVEII	32	7	0
16NR2D8715	J8711	CAD LABORATORY	32	52	1

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

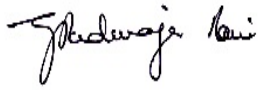
NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **27-12-2017]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

**NOTE:
[-1 in the filed of externals indicates student absent for the respective subject.

-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]



Date:06-12-2017

Controller of Examinations